

Lecture 4

Applications of Operational Amplifiers

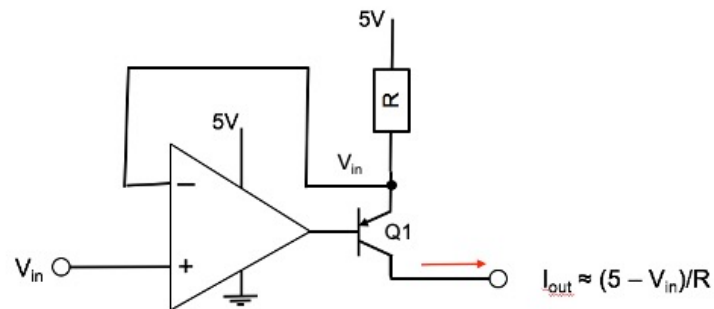
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In this week's lecture, I will be exploring a number of applications using op-amp as building blocks. These are commonly used circuits, some of which you have already come across in Year 1, either in the Analysis and Design of Circuits module or in the practical work.

To support this lecture, you will also be building and testing most of the circuits explored in this lecture in Laboratory Experiment 2 this week.

Voltage to current converter



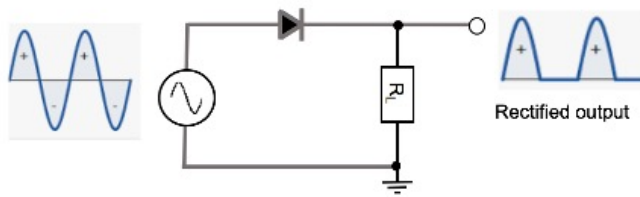
- ❖ PNP transistor Q1 must be in linear region
- ❖ Op-amp forces $V_- = V_{in}$
- ❖ R (with 5V) determines the current as $I_R = (5 - V_{in})/R$
- ❖ Assume no current flows into input of op-amp
- ❖ $I_C = I_E - I_B$, assume current gain $\beta \gg 1$, $I_C \approx I_E \approx I_R$
- ❖ Can use FET or MOSFET in place of BJT

We can convert a voltage V_{in} to a current I_{out} that is proportional to the voltage with high accuracy with this circuit. The PNP transistor Q1 MUST BE working in the linear region at all times. The op-amp's negative feedback forces the voltage at V_- to V_{in} . The resistor R determines the current flowing into the emitter of Q1. Assuming that the current gain of Q1 is relatively large (say at least 100), then $I_{out} = I_C \approx I_E$.

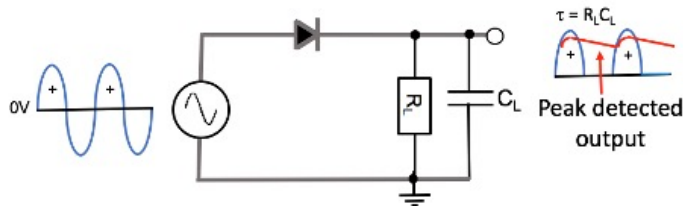
The output current is independent of the collector voltage of Q1. Therefore this is a good current source.

Instead of using a BJT, one could use either a p-channel FET or MOSFET instead.

Half-wave rectifier & Peak detector



- ❖ Diode and resistor – simple half-wave rectifier
- ❖ Commonly used in power electronics or and multimeters



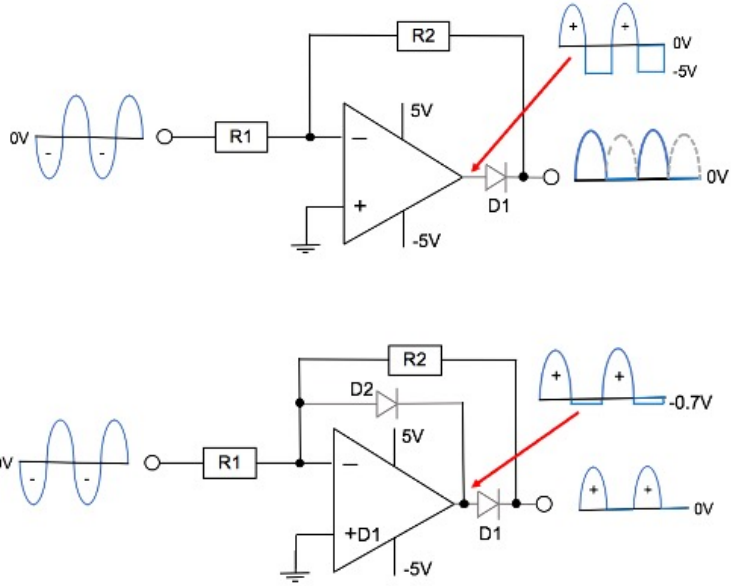
- ❖ C_L charges to V_{in} peak $- V_D$
- ❖ Diode prevents C_L discharging when V_{in} drops
- ❖ R_L discharges capacitor with time constant $R_L C_L$
- ❖ C_L charges again on the positive cycle

You are familiar with how diodes work. Here is a simple rectifier circuit using a single diode. Only the positive going half cycle of the input sine wave will forward bias the diode for current to flow from the source to R_L . On the negative half cycle, the diode is reverse biased and no current (except leakage current) flows to the load.

Such rectifier circuit is commonly used in power supply circuits to convert 50Hz (60Hz in North America) mains voltage to DC. You will learn more about such power conversion circuits next term on the Power Electronics module. You will also find similar circuit in a multimeter, which converts the measured ac signal to dc either through averaging (lowpass filtering) or through peak detection.

Adding a capacitor in parallel to R_L results in a peak detector circuit. The capacitor charges to when $V_{in} \geq V_C + V_D$ through the diode which is forward biased. When $V_{in} < V_C + V_D$, the diode is no longer forward biased. The capacitor discharges through the load resistors R_L . This peak detector circuit produces an output that is roughly a DC voltage but it contains ripple. The size of the ripple is dependent on the time constant $R_L C_L$ and the frequency of the input signal. For the peak detector to work effectively $R_L C_L \gg$ period of the signal (e.g. $R_L C_L = 10 / F_s$, where F_s is the signal frequency).

Rectifier with op-amp buffering



- ❖ Assume $R1 = R2$
 - ❖ Negative cycles result in an inverting amplifier with gain = -1
 - ❖ Op-amp drives output with low impedance
 - ❖ Positive cycles, op-amp isolated from output
 - ❖ Poor full-wave rectification
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- ❖ D1 provides feedback path for negative input cycles
 - ❖ D2 provides feedback path for positive input cycles
 - ❖ Op-amp operating throughout entire cycle

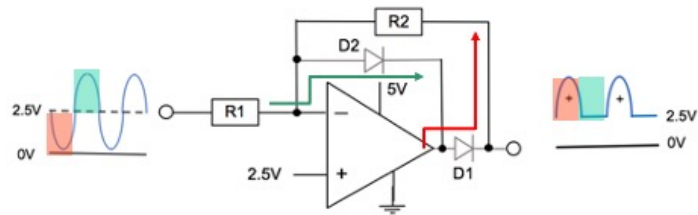
Op-amp can be used to implement a rectifier circuit. Let us assume that we are using a dual $\pm 5V$ supply op-amp, and the reference voltage is GND.

Top circuit uses only one diode. The negative half cycle of the input forces the op-amp output to go positive, forward biasing D1 to complete the feedback loop. This results in a low impedance drive to the output with a positive voltage as shown.

On the positive half cycle of the input, the op-amp output goes negative reverse biasing D1. Now the feedback loop is broken by the diode. The op-amp output goes to -5V. The V- input is no longer virtual earth at GND potential. The output is now driven through R1 and R2. The voltage at the output will be the same as the positive input signal, but subject to the loading effect.

A somewhat better circuit is shown below. Here we add another diode D2. This provides feedback path for the positive half of the input signal. The result is a half-wave rectifier with the output always driven by the op-amp whose V- input is forced to be at virtual earth GND voltage.

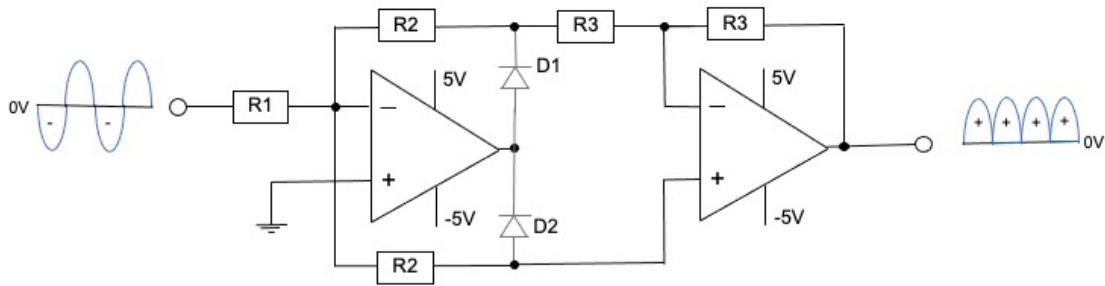
Single power supply “rectifier”



- ❖ Single power supply rectifier is implemented by shifting the reference voltage to $\frac{1}{2} V_{DD}$

Single supply op-amp can also be used as rectifier. Of course “rectification” with only one supply is a bit unusual. Here we lift the reference voltage from 0V to 2.5V (for $V_{DD} = 5V$), and everything will work as before. However, both input and output are now relative to the 2.5V offset.

Full-wave rectifier



- ❖ Precision full-wave rectifier with two op-amps
- ❖ Op-amp 1 provides two separate half of the rectified signals
- ❖ Op-amp 2 sums two half cycles together

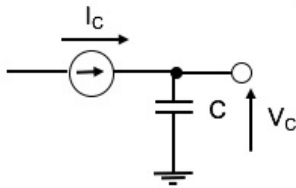
A full-wave rectifier that can drive an output load effectively can be implemented with two op-amps.

The two paths through D1 and D2 provide negative feedback for negative and positive half cycle of the input respectively.

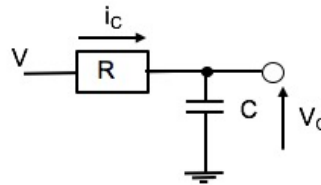
The second op-amp acts as a summing circuit that adds the two half together to provide a full-wave rectified output.

Integrator

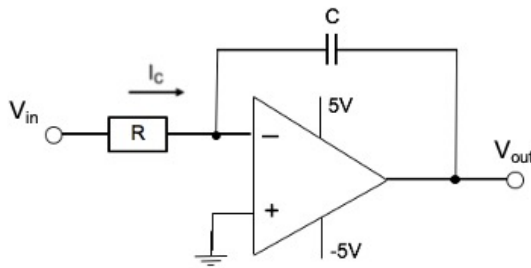
$$i_C = C \frac{dV_C}{dt} \Rightarrow V_C = \frac{1}{C} \int i_C dt + V_C(0)$$



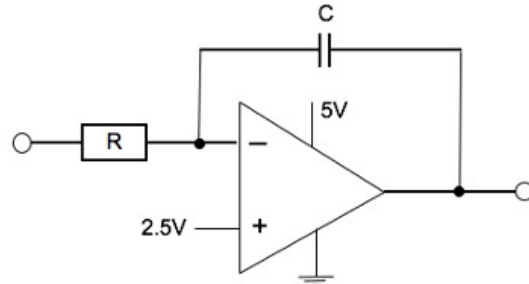
❖ Constant i_C , $V_C = \frac{i_C}{C} t + V_C(0)$



- ❖ i_C changes with V_C
- ❖ V_C is an exponential rise function (not perfect integral)



❖ $v_{out} = -\frac{V_{in}}{RC} t + V_C(0)$



- ❖ Single supply operation

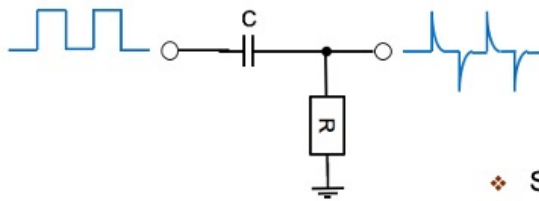
If we have an ideal constant current source, a capacitor will integrate the current perfectly to produce $V_C(t)$. $V_C(0)$ is the initial capacitor voltage.

One could use a resistor to convert voltage V to a current to charge the capacitor. This of course will not produce a very good integrator because the current charging the capacitor is no longer constant. As the capacitor charges up, V_C increases and i_C decreases. $V_C(t)$ follows the exponential rise function.

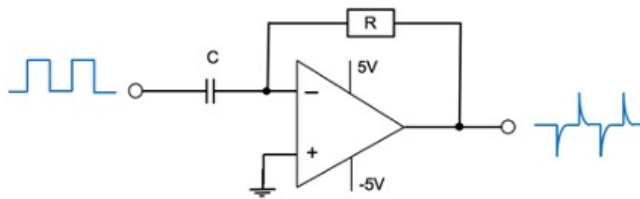
We can implement a near perfect integrator using an op-amp as shown on the slide. The inverting op-amp has V^- node fixed as virtual earth, and R is now used to convert V_{in} to a current $i_C = V_{in}/R$. The current has nowhere to go except to charge capacitor C .

Implementing an op-amp integrator using single power supply is again straight forward. The virtual earth node is now a virtual 2.5V, which is the reference voltage for the circuit.

Differentiator



- ❖ Swap R and C
- ❖ Implement a differentiator
- ❖ Not used often because circuit tends to produce noisy output

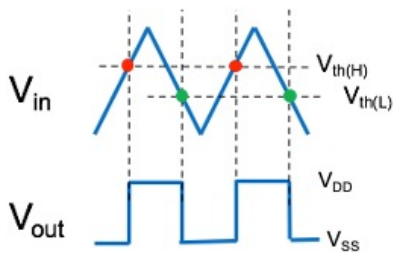
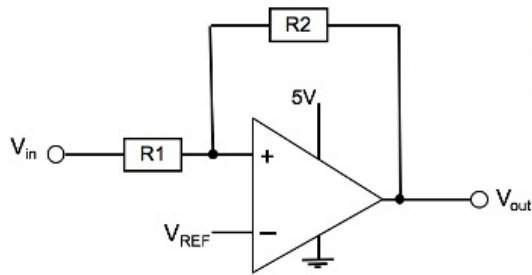


Swapping R and C in both passive and op-amp circuit for the two circuits as integrators yields two differentiator circuits. Both provide an approximation to the differentiation function as shown.

The way it works is that the voltage across a capacitor cannot change instantaneously. Therefore the output follows the change in input before the capacitor charges (or discharges).

Differentiator circuits are not popular. It tends to amplify high frequency signals and produces a very noisy output which makes them not useful in practical applications.

Comparator with hysteresis



- ❖ V_{out} swings between V_{DD} and V_{SS}
- ❖ V_{out} changes state when V_+ reaches V_{REF}
- ❖ Apply KCL at V_+ :

$$\frac{V_{REF} - V_{in}}{R1} = \frac{V_{out} - V_{REF}}{R2}$$

$$\Rightarrow V_{in} = V_{REF} \left(1 + \frac{R1}{R2} \right) - V_{out} \left(\frac{R1}{R2} \right)$$

- ❖ If $R1 = 0$ or $R2 = \infty$, $V_{th} = V_{REF}$
- ❖ $R1 > 0$, $R2 \neq \infty$

$$V_{th(H)} = V_{REF} \left(1 + \frac{R1}{R2} \right) - V_{SS} \left(\frac{R1}{R2} \right)$$

$$V_{th(L)} = V_{REF} \left(1 + \frac{R1}{R2} \right) - V_{DD} \left(\frac{R1}{R2} \right)$$

- ❖ Hysteresis = $V_{th(H)} - V_{th(L)}$

Op-amp can be used as an analogue comparator. In the circuit shown, V_{REF} is constant voltage that defines the comparator threshold for switching output from high (V_{DD}) to low (V_{SS}) voltages. V_{out} changes state when V_+ reaches V_{REF} from either direction (i.e. with V_{in} rising or falling).

Applying KCL at V_+ node yields the equation for V_{in} when switching occurs:

$$V_{th} = V_{REF} \left(1 + \frac{R1}{R2} \right) - V_{out} \left(\frac{R1}{R2} \right)$$

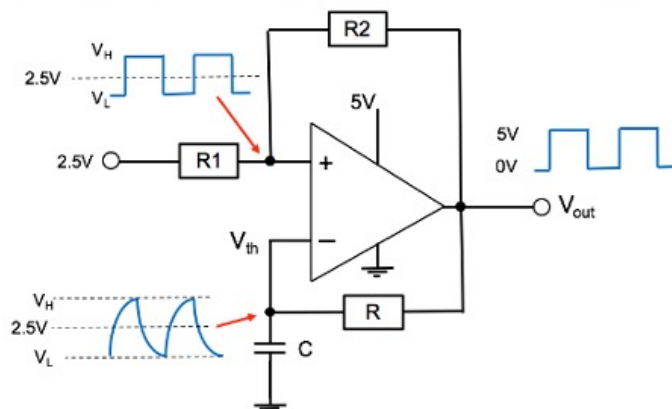
If $R1 = 0$ or $R2$ is open circuit, the $V_{th} = V_{REF}$.

If the op-amp has high gain-bandwidth product and high output slew rate (i.e. the maximum rate of change of the output voltage), the switching condition of $V_{th} = V_{REF}$ could result in output oscillation if V_{in} is changing slowly.

With $R1 > 0$ and $R2 < \infty$, the switching threshold is dependent on the state of V_{out} . Therefore the switching threshold when the signal is rising is different from that when the signal is falling. This creates the hysteresis effect.

This circuit is also known as a **Schmitt trigger** circuit.

Simple Oscillator



- ❖ Combine comparator with hysteresis and RC network = oscillator
- ❖ Voltage at V+ change instantly with V_{out}:

$$V_H = 2.5 \left(1 + \frac{R1}{R1+R2} \right)$$

$$V_L = 2.5 \left(\frac{R2}{R1+R2} \right)$$

- ❖ V₋ = V_{th} rises and falls exponentially with a time constant of RC between V_H and V_L
- ❖ This is determined by the equation:

$$V_{th} = V_f + (V_i - V_f)e^{-\frac{t}{\tau}}$$

V_i = initial value, V_f = final value, τ = time constant RC

This shows a simple square wave oscillator circuit. Assume V_{out} is oscillating between V_{DD} = 5V and V_{SS} = 0V. For the given circuit, V+ node voltage changes instantly with V_{out} between V_H and V_L as shown (simple voltage divider).

However, V- node cannot change instantaneously because of C. Instead, the voltage V_{th} follows an exponential rise and fall equation.

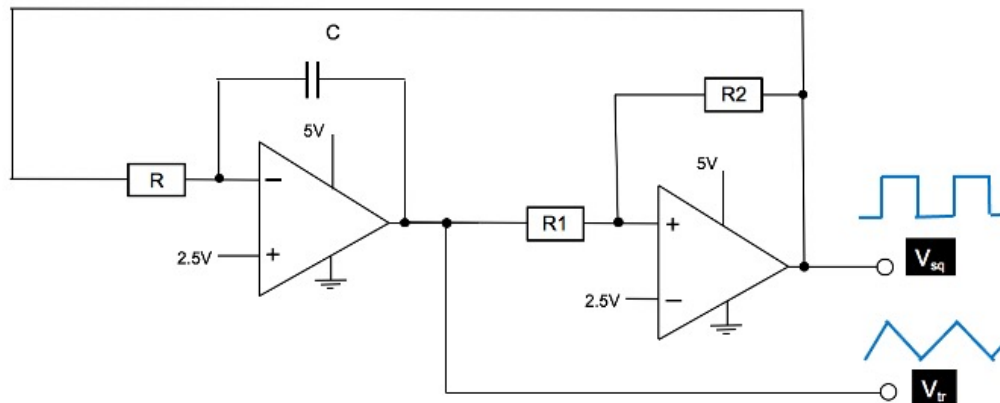
In general, for a C that is charged or discharged from a voltage source through a resistor R, the capacitor voltage is given by the equation:

$$V_C = V_f + (V_i - V_f)e^{-\frac{t}{\tau}}$$

where V_i and V_f are the initial and final values of the voltage V_C respectively and τ is the time constant RC.

For the rising portion of V_{th}=V_C, V_i = V_L and V_f = 5. For the fall portion of V_{th}, V_i = V_H and V_f = 0.

Triangular and Square wave generator

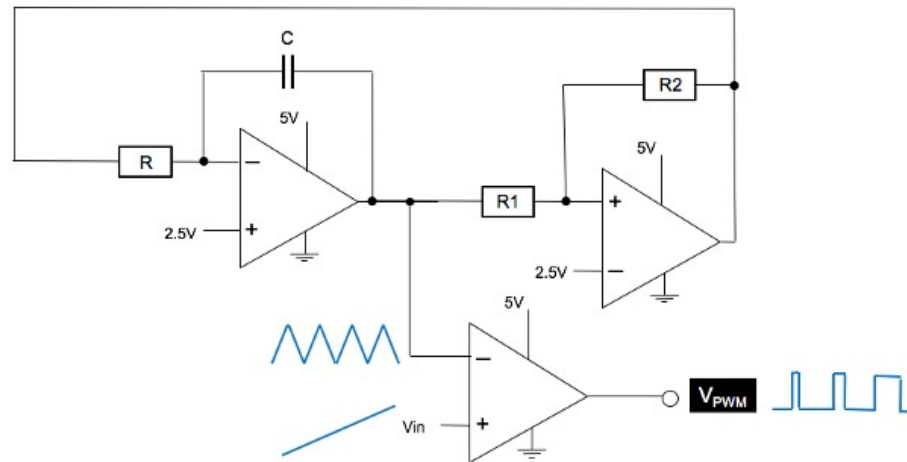


- ❖ Better oscillator circuit using integrator + comparator with hysteresis
- ❖ Integrator output produces a triangular signal
- ❖ Comparator (with hysteresis) produces a square signal
- ❖ Feedback circuit ensures oscillation is maintained

This oscillator generates both a triangular signal and a square signal at the same time. It uses an op-amp integrator to produce a negative going ramp when the integrator input is at V_{DD} . It produces a positive going ramp when the integrator input is at V_{SS} or 0V.

Since the comparator is designed to have hysteresis, the triangular signal causes the comparator to switch state when $V_{th(H)}$ and $V_{th(L)}$ are reached. (See slide 9.)

Pulse-width Modulator



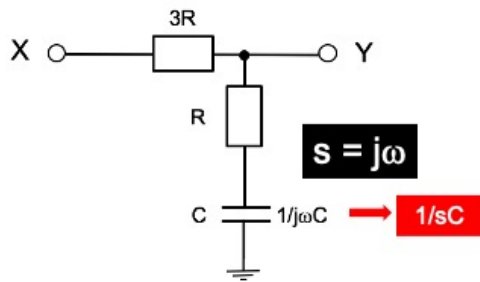
- ❖ Comparing triangular signal with V_{in} -> pulse-width modulated output
- ❖ Frequency of triangular signal $\gg V_{in}$ frequency
- ❖ Output pulse width proportional to value of V_{in}
- ❖ Recover V_{in} by lowpass filtering V_{PWM}

We can implement a pulse-width modulator by simply comparing the input signal V_{in} to the periodic triangular signal. The output is a sequence of pulses whose widths are proportional to the value of V_{in} . For this to work, the frequency of the triangular signal must be much higher than that of the input signal V_{in} .

You will find PWM circuits in many devices, particularly in microcontrollers. We will also be examining how to produce PWM signals in digital circuits later in this module.

Pulse-width modulated signal is very useful in power electronics where we want to obtain an average voltage through switching transistors ON and OFF. PWM signal is also commonly used to control speed of motors. When a transistor (BJT, FET or MOSFET) is used as a switch (instead of a linear device), the the switch resistance is low when the current is high during the ON state, and the resistance is very high, but the current is low during the OFF state. Therefore the power dissipated (or wasted) by a transistor controlled by a PWM signal is low. This leads to higher efficient in the system.

Transfer Function of 1st order LP Filter



- ❖ More general if use **complex frequency s** to represent the quantity $j\omega$
- ❖ Covered in Signals and Systems module this term, and Control module next term
- ❖ Express impedance of capacitor as $1/sC$ instead of $1/j\omega C$
- ❖ Capture both steady state (ac) and transient behaviour

❖ Year 1 ADC Part 1 Lecture 11, slide 3

❖ Transfer function defined as: $H(s) = \frac{Y(s)}{X(s)} = \frac{R+1/sC}{4R+1/sC} = \frac{1+sRC}{1+4sRC}$

❖ Frequency response is calculated as $H(s)|_{s=j\omega} = \frac{Y(j\omega)}{X(j\omega)} = \frac{1+j\omega RC}{1+4j\omega RC}$

❖ Easier to perform algebra manipulation than using $j\omega$

❖ Provides better intuitions on system behaviour

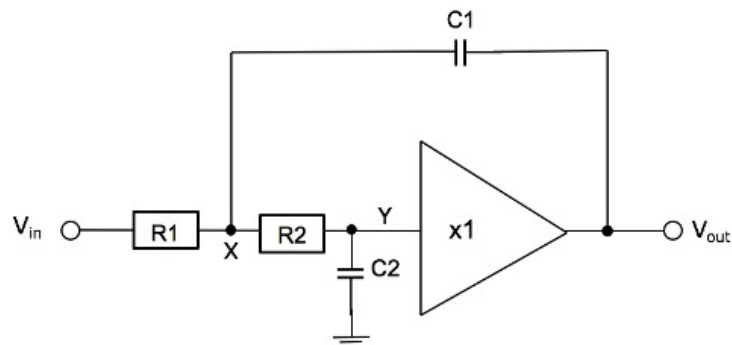
Consider the simple RC network shown. This was analysed in Year 1 ADC Lecture 11 (slide 3) already. However, in this case, we substitute s for $j\omega$. The variable s is known as “**complex frequency**”. You will learn about this in two other modules: Signals and Linear Systems, and in Control Engineering.

The reason s is used in preference to $j\omega$ because frequency response $H(j\omega)$ is only valid if the circuit (or system) is in steady state (i.e. all transients have died down) and all signals are expressed as sine waves. Using complex frequency s allows both transient and steady state behaviours to be analysed.

The impedance of a capacitor is $1/sC$ instead of $1/j\omega C$.

Furthermore, you will learn in other modules the relationship between the transfer function $H(s)$ expressed as products of factors in s , and how this relates to the idea of poles and zeroes. (This is outside the scope of this module.)

Sallen-Key 2nd order lowpass filter (1)



❖ $Y = V_{out}$ apply KCL at node X, and obtain transfer function in s as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R1C1R2C2} \times \left[\frac{1}{s^2 + s \left(\frac{1}{R2C1} + \frac{1}{R1C1} \right) + \frac{1}{R1C1R2C2}} \right]$$

Op-amps are often used to build active filters. Here is a common active filter using the **Sallen-Key** architecture. This filter is popular because it is easy to understand and to analyse, uses non-inverting amplifier (which in this case is a unity gain buffer), requires only Rs and Cs (no inductors), and can implement highpass, lowpass or bandpass filters with cascaded stages.

Using complex frequency s and apply KCL to node X shown here, we can derive the transfer function $H(s)$ as shown.

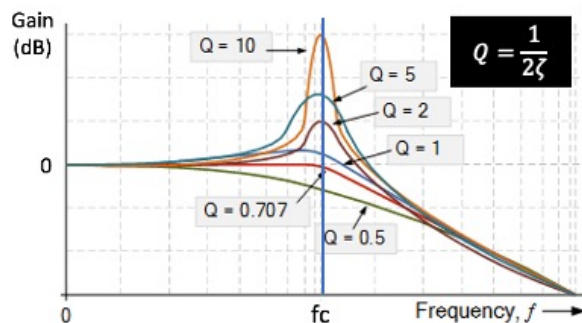
Sallen-Key 2nd order lowpass filter (2)

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R_1 C_1 R_2 C_2} \times \left[\frac{1}{s^2 + s \left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_1} \right) + \frac{1}{R_1 C_1 R_2 C_2}} \right]$$

❖ Cut-off frequency f_c is:

$$H(s) = (2\pi f_c)^2 \times \left[\frac{1}{s^2 + 2\zeta(2\pi f_c) s + (2\pi f_c)^2} \right]$$

$$H(s) = G_0 \times \left[\frac{1}{s^2 + a_1 s + a_0} \right]$$



- ❖ a_0 determines the **cut-off frequency** of filter
- ❖ a_1 determines the **resonance behaviour** of filter
- ❖ G_0/a_0 is the **gain of the filter at dc**
- ❖ **Butterworth filter:** $2\zeta = 1.414$, $Q = \frac{1}{2\zeta} = 0.707$
- ❖ **Maximally flat** gain in passband
- ❖ **Monotonically decreasing** gain in stop band

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Substituting $s = j\omega = 0$, $H(0) = \text{DC gain} = 1$ for this filter. Furthermore, the cut-off (break) frequency is given by the equation above.

The transfer function $H(s)$ can be written in terms of the cut-off frequency f_c and the damping factor ζ as shown in the slide. Since this is a 2nd order filter, $H(s)$ can be expressed in a general form with a denominator polynomial in s with a maximum power of 2. There are two coefficients a_1 and a_0 to be chosen (determined by R_1 , R_2 , C_1 and C_2).

The coefficient a_0 is governed by the cut-off frequency of the filter.

$$f_c = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

The only remaining parameter to choose is ζ , which is also called the damping ratio. The quantity $Q = 1/2\zeta$ is known as the quality factor of the filter and it determines how "peaky" the filter is around the cut-off frequency – the higher the Q , the more resonant the filter.

If $2\zeta = 1.414$ (or $Q = 0.707$), the filter is maximally flat, meaning that its gain is 1 until just before cut-off and decreases as frequency increases. This is a class of filters known as **Butterworth filters**.